AMENDMENTS TO THE SPECIFICATION

Please amend the paragraph beginning on page 1, line 1 as follows:

~~DESCRIPTION~~

Please insert the following paragraph on page 1 after the title:

CROSS REFERENCE TO RELATED APPLICATIONS

The present application is a national stage of PCT/JP2004/009169, filed June 30, 2004, which claims priority to Japanese application No. 2003-295386, filed August 19, 2003.

Please amend the paragraph beginning on page 1, line 4 as follows:

~~Technical~~ Field of the Invention

Please amend the paragraph beginning on page 1, line 9 as follows:

Background ~~Art~~ of the invention

Please amend the paragraph beginning on page 1, line 10 as follows:

Japanese Unexamined Patent Application Publication No. 60-192401 ("Patent Document 1") discloses a line transition including a planar circuit formed using a dielectric substrate and a solid waveguide for propagating electromagnetic waves in a three-dimensional space to realize planar-circuit to waveguide transition.

Please amend the paragraph beginning on page 2, line 6 as follows:

~~Patent Document 1: Japanese Unexamined Patent Application Publication No. 60-192401~~

Please amend the paragraph beginning on page 2, line 8 as follows:

~~Disclosure of the Invention~~

Please amend the paragraph beginning on page 2, line 20 as follows:

(1) Impedance of a short-circuit portion in the waveguide (the short-circuit structure including a structure using the cut-off characteristics of the waveguide); and

Please amend the paragraph beginning on page 2, line 24 as follows:

(2) Impedance of a portion (edge of the dielectric substrate), where the microstrip line does not exist in the dielectric substrate, in the waveguide.

Please add the following after the paragraph beginning on page 4, line 14 as follows:

Summary of the Invention

Please amend the paragraph beginning on page 5, line 3 as follows:

The present invention provides a line transition including a solid waveguide and a planar circuit to realize planar-circuit to waveguide transition, the solid waveguide propagating electromagnetic waves within a three-dimensional space, the planar circuit being constructed by forming a predetermined conductive pattern on a dielectric substrate, wherein the dielectric substrate is disposed parallel to the E plane of the solid waveguide in almost the middle of the solid waveguide, the conductive pattern on the dielectric substrate includes a coupled-line pattern segment electromagnetically coupled with a signal propagating through the solid waveguide and a transmission-line pattern segment extending from the coupled-line pattern segment.[[,]] ~~and the~~ The edge of the dielectric substrate has a notch in the vicinity of the coupled-line pattern segment, the notch having a side that is parallel to the signal propagation direction of the coupled-line pattern segment, the length of the side being equal to or longer than the dimension in the width direction of the E plane of the solid waveguide.

Please amend the paragraph beginning on page 7, line 15 as follows:

~~Fig. 1 includes~~ Figs. 1A-1C are diagrams showing the structure of a dielectric substrate used in a line transition according to a first embodiment of the present invention.

Please amend the paragraph beginning on page 7, line 18 as follows:

~~Fig. 2 includes~~ Figs. 2A-2C are diagrams showing the structure of the line transition of the first embodiment.

Please amend the paragraph beginning on page 7, line 23 as follows:

Fig. 4 is a diagram of a motherboard used in manufacturing dielectric substrates for the line transition of the present invention.

Please amend the paragraph beginning on page 8, line 1 as follows:

Fig. 5 is a perspective exploded view of the structure of a line transition according to a second embodiment of the present invention.

Please amend the paragraph beginning on page 8, line 4 as follows:

Fig. 6 is a diagram of the structure of a millimeter-wave radar module including the line transition according to the first embodiment of the present invention.

Please amend the paragraph beginning on page 8, line 7 as follows:

~~Best Mode for Carrying Out~~ Detailed Description of the Invention

Please amend the paragraph beginning on page 8, line 8 as follows:

A line transition according to a first embodiment and a method for manufacturing the line transition will now be described with reference to Figs. 1A to 4.

Please amend the paragraph beginning on page 8, line 11 as follows:

~~Fig. 1 shows~~ Figs. 1A through 1C show the structure of a dielectric substrate serving as a component of the line transition. ~~(A)~~ Fig. 1A is a top view of the dielectric substrate, ~~(B)~~ Fig. 1B is a bottom view thereof, and ~~(C)~~ Fig. 1C is an enlarged view of a portion shown by a broken line in ~~(B)~~ Fig. 1B. On the upper surface of a dielectric substrate 3, a ground conductor 21, chip connection electrodes 22 to 26, and external

connection terminals 27 to 29 are formed. Terminals of a chip 8 are soldered to the chip connection electrodes 22 to 26, respectively.

Please amend the paragraph beginning on page 8, line 21 as follows:

As shown in Fig. 1B ~~(B)~~, on the lower surface of the dielectric substrate 3, a ground conductor 11, transmission-line conductors 14a and 15a, coupled-line conductors 14k and 15k, transmission-line conductors 16, 17a, and 17b are formed. The coupled-line conductors 14k and 15k each correspond to a coupled-line pattern segment.

Please amend the paragraph beginning on page 9, line 21 as follows:

~~Fig. 2 shows~~ Figs. 2A through 2C show the structure of the line transition of the present invention. To show the surface on which the coupled-line conductors are formed, the line transition is turned upside down. ~~(A)~~ Fig. 2A is a top view of the line transition, of which a lower conductive plate is omitted, ~~(B)~~ Fig. 2B is a sectional view of the line transition at the line B-B in Fig. 2A ~~(A)~~, and ~~(C)~~ Fig. 2C is a sectional view thereof at the line C-C in Fig. 1A ~~(A)~~. Fig. 3 is a partial perspective view of the positional relationship between two upper and lower dielectric strips and the dielectric substrate.

Please amend the paragraph beginning on page 11, line 3 as follows:

As shown in Figs. 1A and 1B ~~Fig. 1~~, the ground electrode 21 is not formed (a space is provided) on the rear surface (upper surface of the dielectric substrate 3) of the portion where the coupled-line conductor 14k is formed, the surface facing the lower conductive plate 1. This space functions as a suspended line. The suspended line is electromagnetically coupled with the propagating mode of the waveguide including the dielectric strips 6 and 7 and the conductive plates 1 and 2.

Please amend the paragraph beginning on page 11, line 13 as follows:

In the lower conductive plate 1, as shown in ~~(C) of~~ Fig. 2C, a groove G12 for the transmission line is formed along the coupled-line conductor 14k and the transmission-line conductor 14a on the dielectric substrate 3. The transmission-line groove G12 provides a

predetermined space adjacent to the microstrip line on the side of a signal line and also shields against another mode such as a higher order mode. A choke groove G22 is formed in the upper conductive plate 2. The conductive plate 1 with the above structure is superposed on the conductive plate 2 with the above structure, thus reducing radiation loss from a gap in the interface between the plates.

Please amend the paragraph beginning on page 12, line 8 as follows:

A signal supplied from the external connection terminal 27 shown in Fig. 1A is propagated to the connection conductor 24 through the transmission-line conductor 16. According to the present embodiment, the chip 8 in Fig. 1A includes a x2 multiplier MLT, amplifiers AMPa and AMPb, a directional coupler CPL, and an amplifier AMPc.

Please amend the paragraph beginning on page 13, line 15 as follows:

Fig. 4 shows a motherboard to be cut into dielectric substrates 3. In Fig. 4, broken lines VL0 to VL4' and HL0 to HL4 indicate dicing lines of a motherboard 30. The conductive pattern shown in Fig. 1A is formed on each of workpieces obtained by cutting the motherboard along the vertical and horizontal dicing lines. Through holes H1 and H2 are formed between each workpiece and adjacent workpieces. Referring to Fig. 4, the dicing line VL3 passes through the through hole H1 formed between a right upper dielectric-substrate workpiece 3' and the adjacent dielectric-substrate workpiece on the left. The dicing line HL1 passes through the through hole H2 between the dielectric-substrate workpiece 3' and the adjacent lower dielectric-substrate workpiece.

Please amend the paragraph beginning on page 14, line 3 as follows:

The shrinkage rate of the motherboard 30 to be fired relatively remarkably varies depending on various parameters. The sizes of the through holes H1 and H2 are determined such that the respective dicing lines pass through formation areas of the corresponding through holes H1 and H2 even when the shrinkage rate is the highest relative to the design center or the lowest relative thereto. Thus, the spacing (da in ~~(C) of~~ Fig. 1C) between the notch N1 and the coupled-line conductor 14k and that between the

notch N2 and the coupled-line conductor 15k in Fig. 1B can always be made uniform. Although the spacing da varies depending on the shrinkage rate of the motherboard 30, the spacing da is not influenced by the relative displacement of the dicing lines with respect to the motherboard 30. Accordingly, the variation in the spacing da presents no problem.

Please amend the paragraph beginning on page 15, line 7 as follows:

The chip 8 shown in Fig. 1A is mounted on each dielectric substrate 3.

Please amend the paragraph beginning on page 15, line 9 as follows:

After that, as shown in Figs. 2A, 2B, 2C and 3, the dielectric strips 6 and 7 are fitted into the grooves of the lower and upper conductive plates 1 and 2, respectively. After that, the dielectric substrate 3 is disposed between the lower and upper conductive plates 1 and 2.

Please amend the paragraph beginning on page 15, line 15 as follows:

When the frequency of a transmission signal is within the 76-GHz band, respective dimensions in ~~Figs. 1 and 2~~ Figs. 1A, 1B, 1C, 2A, 2B and 2C are as follows: